Ange-Thierry Ishimwe

ange-thierry.ishimwe@colorado.edu — +1 (479) 320-9300 — linkedin.com/in/ange-thierry-ishimwe-202082139

SUMMARY

PhD Graduate and researcher in CPU microarchitecture and security. My work spans hardware defenses against transient execution attacks, compiler enhancements for memory safety, and machine-learning–driven optimizations for code synthesis. I have extensive experience with the Gem5 simulator (C++/OOP and Python), Clang/LLVM compiler, and FPGA programming on Zynq platforms using Verilog/SystemVerilog and Vivado.

WORK EXPERIENCE

Graduate Research Assistant Aug 2020 – May 2026

University of Colorado Boulder, Boulder, CO

- Designed SSMR, a software–hardware co-design defense against Spectre and Meltdown that extends the load–store unit to detect unsafe speculative memory operations based on their target addresses.
- Realized SSMR through Clang/LLVM passes (C++) that identify expected memory operations at compile time and encode this metadata into custom RISC-V instructions, and at the microarchitectural level designed a hardware buffer for this instruction metadata in Gem5, enabling the CPU to distinguish between safe and unsafe accesses.
- Designed and implemented a machine learning–based pruning strategy for Souper, a synthesis-driven superoptimization compiler, by creating a custom dataset, training the model on the dataset in Python, and deploying it in the C++ codebase of Souper via ONNX Runtime for inference.
- Developed a functional-level model of AMD's Speculative Store Bypass Predictor(SSBP) in Gem5 and evaluated SCPC, a defense that isolates predictor state across processes and privilege levels to prevent cross-domain attacks.

Undergraduate Research Assistant August 2019 – May 2020

University of Arkansas, Fayetteville, AR

- Aided in designing and building a custom accelerator in Verilog for IoT edge devices that accelerates matrix and vector operations for machine learning workloads. Using a Zynq FPGA board, we achieved 24.51× speedup over an HLS-based design and 1.75× over prior custom implementations on RNN and LSTM benchmarks.

RELEVANT PROJECTS

Python-to-x86 Compiler

- Built a multi-pass compiler that translates a subset of Python code into x86 assembly, implementing the complete compilation pipeline from parsing through code generation.
- Implemented dataflow analyses and backend optimizations including liveness analysis, interference graph construction, graph-coloring register allocation, and spill code insertion.
- Developed support for functions, closures, classes, inheritance, and polymorphic types while generating executable x86 assembly code.

EDUCATION

University of Colorado Boulder

PhD, Electrical and Computer Engineering 2022 – 2026

MS, Electrical and Computer Engineering (GPA: 3.76/4.0) 2020 – 2022

University of Arkansas

BS, Computer Engineering (GPA: 3.6/4.0) 2016 – 2020

SKILLS

Clang/LLVM, Gem5, Vivado, C/C++, Python, Verilog/SystemVerilog, Assembly (RISC-V, x86, ARM), Cacti

PUBLICATIONS

- **Ishimwe**, McDiarmid-Sterling, McKevitt, Lehman. "SSMR: Statically Detecting Speculation Safe Memory Regions to Mitigate Transient Execution Attacks." *CC 2026.*
- Thomas, Workneh, **Ishimwe**, McKevitt, Curlin, Bahar, Izraelevitz, Lehman. "Baobab Merkle Tree for Efficient Secure Memory." *CAL 2024.*
- Panahi, Balsalama, **Ishimwe**, Mbongue, Andrews. "A Customizable Domain-specific Memory-centric FPGA Overlay for Machine Learning Applications." *FPL 2021.*